UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/808,114	03/15/2001	Leonard Forbes	M4065.0381/P381	3126

24998 7590 06/19/2003

DICKSTEIN SHAPIRO MORIN & OSHINSKY LLP
2101 L STREET NW
WASHINGTON, DC 20037-1526

EXAMINER
QUINTO, KEVIN V

ART UNIT	PAPER NUMBER
2826	

DATE MAILED: 06/19/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/808,114	FORBES ET AL.	
	Examiner	Art Unit	
	Kevin Quinto	2826	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *04 April 2003* .

2a)☒ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-91* is/are pending in the application.

4a) Of the above claim(s) *68-91* is/are withdrawn from consideration.

5)☒ Claim(s) *1-16 and 33-41* is/are allowed.

6)☒ Claim(s) *17, 42, 54-58* is/are rejected.

7)☒ Claim(s) *18-32,43-53 and 59-67* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

NATHAN J. FLYNN
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2800

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Response to Arguments

1. Applicant's arguments with respect to claims 17-32, 43-53, and 54-67 have been considered but are moot in view of the new ground(s) of rejection.

2. The applicant's amendment has overcome the rejection of claims 33-41 under 35 USC § 112.

3. In view of the amendment made to claim 37, the examiner hereby withdraws the objection made to claim 37.

Claim Objections

4. Claim 57 is objected to because of the following informalities: the word ***type*** is misspelled as "tope." Appropriate correction is required.

Claim Rejections - 35 USC § 102

5. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

6. Claims 17 and 42 are rejected under 35 U.S.C. 102(e) as being anticipated by Shin et al. (USPN 6,563,151 B1).

7. In reference to claim 17, Shin et al. (USPN 6,563,151 B1, hereinafter referred to as the "Shin" reference) discloses a similar device. Figures 2 and 3 both illustrate a semiconductor transistor with three gate electrodes. The substrate (501, 701) has at least two spaced doped source/drain regions (505, 705) which defines a channel between them. There is a gate dielectric (509, 709) over the substrate. The central gate electrode (511, 711) contains a first dopant (511 contains p+, 711 contains n+) and is over the gate dielectric (509, 709) and the channel. There are two outer gate electrodes (515, 715) over the gate dielectric (509, 709) and the channel. The outer gate electrodes (515, 715) contain a second dopant (515 contains n+, 715 contains p+) which is different than the first dopant of the central gate electrode (511 contains p+, 711 contains n+). The outer gate electrodes (515, 715) are separated from the central gate electrode (511, 711) by a dielectric layer (513, 713). The workfunction difference between the central gate electrode (511, 711) and the outer gate electrodes (515, 715) is such that the central gate electrode (511, 711) experiences a greater threshold voltage than the outer gate electrodes (515, 715).

8. In reference to claim 42, Shin (USPN 6,563,151 B1) discloses a similar device. Figures 2 and 3 both illustrate a semiconductor transistor with three gate electrodes. The substrate (501, 701) has at least two spaced doped source/drain regions (505, 705) which defines a channel between them. There is a gate dielectric (509, 709) over the substrate. The central gate electrode (511, 711) is over the gate dielectric (509, 709)

and the channel. There are two outer gate electrodes (515, 715) over the gate dielectric (509, 709) and the channel. The outer gate electrodes (515, 715) are separated from the central gate electrode (511, 711) by a dielectric layer (513, 713). The gate dielectric (509, 709) has a thickness which is the same under the outer gate electrodes (515, 715) and the central gate electrode (511, 711). The workfunction difference between the central gate electrode (511, 711) and the outer gate electrodes (515, 715) is such that the central gate electrode (511, 711) experiences a greater threshold voltage than the outer gate electrodes (515, 715).

Claim Rejections - 35 USC § 103

9. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

10. Claims 54 and 56 are rejected under 35 U.S.C. 103(a) as being unpatentable over Boyd et al. (USPN 5,895,487) in view of Shin et al. (USPN 6,563,151 B1) and further in view of Choi (USPN 6,072,210).

11. With regard to claim 54, Boyd et al. (USPN 5,895,487, hereinafter referred to as the "Boyd" reference) discloses (in figure 3) a processor which is coupled to a DRAM memory device. Boyd does not disclose the use of a transistor with three gate electrodes in the DRAM memory device. However transistors with three gate electrodes are well known in the art. Shin (USPN 6,563,151 B1) discloses a submicron

semiconductor transistor with three gate electrodes in figures 2 and 3. The substrate (501, 701) has at least two spaced doped source/drain regions (505, 705) which defines a channel between them. There is a gate dielectric (509, 709) over the substrate. The central gate electrode (511, 711) is over the gate dielectric (509, 709) and the channel. The central gate electrode (511, 711) contains a first dopant (511 contains p+, 711 contains n+) and is over the gate dielectric (509, 709) and the channel. There are two side gate electrodes (515, 715) over the gate dielectric (509, 709) and the channel. The side gate electrodes (515, 715) contain a second dopant (515 contains n+, 715 contains p+) which is different than the first dopant of the central gate electrode (511 contains p+, 711 contains n+). The side gate electrodes (515, 715) are separated from the central gate electrode (511, 711) by an insulating dielectric layer (513, 713). The gate dielectric (509, 709) has a thickness which is the same under the outer gate electrodes (515, 715) and the central gate electrode (511, 711). Shin does not disclose using the device in figures 2 and 3 in a DRAM. However Choi (USPN 6,072,210) discloses that submicron features are desirable in a DRAM since it provides a high density DRAM (column 1, lines 10-12). The transistors in figures 2 and 3 of Shin have submicron channels. In view of Choi, it would therefore be obvious to use the transistors of Shin in the DRAM of Boyd.

12. With regard to claim 56, Shin discloses the use of metal (column 7, lines 3-6, 65-67 and column 8, lines 1-2) for the central gate (511, 711) such that the workfunction is higher than the side gate electrodes (515, 715).

13. Claims 54, 55, 57, and 58 are rejected under 35 U.S.C. 103(a) as being unpatentable over Boyd et al. (USPN 5,895,487) in view of Mandelman et al. (USPN 6,097,070).

14. With regard to claim 54, Boyd (USPN 5,895,487) discloses (in figure 3) a processor which is coupled to a DRAM memory device. Boyd does not disclose the use of a transistor with three gate electrodes in the DRAM memory device. However transistors with three gate electrodes are well known in the art. Mandelman et al. (USPN 6,097,070, hereinafter referred to as the "Mandelman" reference) discloses a transistor with three gate electrodes in figure 2. The transistor in figure 2 of Mandelman has a substrate having at least two spaced apart doped source/drain regions (21) with a channel region between them. There is a transistor gate with a central gate electrode (25) on a gate dielectric (27) over the substrate and between the spaced apart doped source/drain regions (21). There are two side gate electrodes (26) located on either side of the central gate electrode (25). The two side gate electrodes (26) are separated from the first gate electrode (25) by an insulating dielectric layer (29). The first gate electrode (25) is of a first conductivity type and the two second gate electrodes (26) are of a second conductivity type. Mandelman discloses that the device is for use in a DRAM memory device (column 5, lines 58-61). Furthermore Mandelman discloses that the device has the benefit of a smaller gate induced drain leakage which leads to better data retention in a DRAM memory device (column 1, lines 30-32). In view of this advantage, it would therefore be obvious to implement the DRAM transistor in the DRAM memory device coupled to the processor of Boyd.

15. With regard to claim 55, there is a conductive cap layer (23) electrically connecting the central (25) and side gate electrodes (26).

16. In reference to claims 57 and 58, Mandelman discloses these conductivity types in figure 2 and in column 4, lines 35-49.

Allowable Subject Matter

17. Claims 1-16 and 33-41 are allowed.

18. Claims 18-32, 43-53, and 59-67 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

19. The following is a statement of reasons for the indication of allowable subject matter: the examiner is unaware of a transistor which has three gate electrodes such that there is a central gate that is surrounded by two side gates where the central gate has a conductive cap layer and the two side gates are electrically connected by another conductive cap layer.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Kevin Quinto whose telephone number is (703) 306-5688. The examiner can normally be reached on M-F 8AM-5PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nathan Flynn can be reached on (703) 308-6601. The fax phone numbers

for the organization where this application or proceeding is assigned are (703) 308-7722 for regular communications and (703) 308-7724 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-0956.

KVQ
June 15, 2003